FOI-R--1519--SE
December 2004
ISSN 1650-1942
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## Final Report December 2004

Sensor Technology
SE-581 11 Linköping

SWEDISH DEFENCE RESEARCH AGENCY

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| Issuing organization | Report number, ISRN | Report type |
|---|---|---|
| FOI – Swedish Defence Research Agency<br>Sensor Technology<br>P.O. Box 1165<br>SE-581 11 Linköping | FOI--1519--SE | Technical report |
| | **Research area code**<br>4. $C^4$ISTAR | |
| | **Month year**<br>December 2004 | **Project no.**<br>I343 |
| | **Sub area code** | |
| | **Sub area code 2** | |



| Author/s (editor/s) | Project manager |
|---|---|
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| | **Approved by**<br>Hans Frennberg |
| | **Sponsoring agency** |
| | **Scientifically and technically responsible**<br>Robert Malmqvist |


**Report title**

Methodology and Technology Studies for Multi-Band and Multi-Standard Wireless Communication in Netwotk Centric warfare – Final Report December 2004


**Abstract (not more than 200 words)**

*To increase knowledge and competence related to methodology and technology for multi-band and multi-standard wireless communication in future network centric warfare, FOI Sensor Technology has participated in a research and development project called "SoCTRix". The SoCTRix project has included participants from both national and international universities, research institutes and private companies. The primary goal of the project has been to demonstrate possibilities to realize a highly integrated and low cost radio transceiver suitable for multi-standard and multi-band wireless communication. In this report, we summarize the main results and conclusions derived from the SoCTRix project. Certain emphasis is given to key areas where FOI has contributed with research and development work. We further discuss possibilities and worldwide trends in using more flexible communication systems in future network centric warfare.*



**Keywords**

Multi-band, multi-standard, wireless communication, network centric warfare, radio transceiver, flexible communication systems.

| Further bibliographic information | Language English |
|---|---|
| **ISSN** 1650-1942 | **Pages** 35 p. |
| | **Price acc. to pricelist** |

| Utgivare | Rapportnummer, ISRN | Klassificering |
|---|---|---|
| Totalförsvarets Forskningsinstitut - FOI | FOI--1519--SE | Teknisk rapport |
| Sensorteknik | **Forskningsområde** | |
| Box 1165 | 4. Ledning, informationsteknink och sensorer | |
| 581 11 Linköping | **Månad, år** | **Projektnummer** |
| | December 2004 | I343 |
| | **Delområde** | |
| | **Delområde 2** | |



| Författare/redaktör | Projektledare |
|---|---|
| Robert Malmqvist | Robert Malmqvist |
| Carl Samuelsson | **Godkänd av** |
| Mattias Alfredson | Hans Frennberg |
| Qamar Ul-Wahab | **Uppdragsgivare/kundbeteckning** |
| | **Tekniskt och/eller vetenskapligt ansvarig** |
| | Robert Malmqvist |


**Rapportens titel (i översättning)**

Studier av metodik och teknik för multi-band och multi-standard trådlös kommunikation i ett nätverksbaserat försvar – Slutrapport December 2004


**Sammanfattning (högst 200 ord)**

*För att öka kunnandet och höja kompetensen kring metodik och teknik för multi-band och multi-standard trådlös kommunikation i ett framtida nätverksbaserat försvar har FOI Sensorteknik deltagit i ett forsknings och utvecklingsprojekt kallat "SoCTRix". SoCTRix-projektet har inkluderat deltagare från såväl universitet och högskolor som institut och företag på både nationell och internationell nivå. Målet med projektet har varit att visa på möjligheter att realisera en högintegrerad lågkostnads radio-transceiver för multi-band och multi-standard trådlös kommunikation. I denna rapport sammanfattas de huvudsakliga resultat och slutsatser som kommit fram ur projektet. Ett visst utrymme i rapporten ges specielt till olika nyckelområden där FOI har bidragit med FoU-insatser. Vi berör även olika möjligheter och trender vad gäller att kunna använda sig av mera flexibla kommunikationssystem i ett framtida nätverksbaserat försvar.*



**Nyckelord**

Multi-band, multi-standard, trådlös kommunikation, nätverksbaserat försvar, radio transceiver, flexibla kommunikationssystems.

| Övriga bibliografiska uppgifter | Språk Engelska |
|---|---|
| **ISSN** 1650-1942 | **Antal sidor:** 35 s. |
| **Distribution enligt missiv** | **Pris: Enligt prislista** |


FOI1004 Utgåva 11 2002.02 www.signon.se Sign On AB

# Contents

# 1. Introduction

## 1.1 Background

Network centric warfare has been adopted as a mean to achieve the information superiority needed in order to assure increased situational awareness in various battlefield scenarios. However, a crucial factor for the successful employment of future network centric warfare is secure access to wireless high capacity data link and communication channels. One reason for this is the relatively large data volumes that one could anticipate have to be transferred between (in certain cases also mobile) sensor nodes that are a part of the combined sensor network. Realizing multi-function radio frequency (RF) sensors that can handle high data rate communication combined with different radar and electronic warfare functions seems, at least from a cost effectiveness point of view, to be a very interesting concept. In order to obtain a high robustness and flexibility for such systems, several different communication standards (protocols) and frequency bands (multi-band) could be used within the sensor network. More specifically, the use of multi-band and multi-standard wireless communication could be advantageous in order to increase the possibilities to circumvent hostile jamming and may also facilitate interoperability at international operations, for example. Which communication protocols and frequency bands that should be used in future sensor networks are however not necessarily totally obvious. Already today, numerous, often incompatible, communication equipments (based on various standards and working in different frequency intervals) are being used by, for example, The Swedish Armed Forces (FM) and others. A possible way out of this dilemma could be to adapt to more flexible communication systems that can be used during both national as well as international missions (for example, in peace-keeping or peace-enforcing operations). The idea of using flexible radio systems seems to be particularly attractive in such cases when certain missions should be accomplished that can be difficult to foresee (and thus plan for) in advance. Trying to combine different standards and frequency bands could finally also be expected to result in challenges related to issues on a system architecture level as well as when it comes to the actual hardware implementation on a sub-system level.

## 1.2 Aim and scope of work

To increase knowledge and competence related to methodology and technology for multi-band and multi-standard wireless communication in future network centric warfare, FOI Sensor Technology has joined a research and development project called “SoCTRix” managed by the Swedish Microelectronic Institute Acreo. The primary goal of the project is to demonstrate possibilities to realize a highly integrated and low cost radio transceiver suitable for multi-standard and multi-band wireless communication. This report can essentially be divided into two different parts. The first part treated in chapter 2 covers possibilities and worldwide trends in using more flexible communication systems such as Software Defined Radio (SDR), for example, in future network centric warfare. The second part, finally, described in chapter 3, presents an over-view of the SoCTRix project with certain emphasis given to key areas within the project where FOI has contributed with research and development work.

## 1.3 List of activities performed within the project

As a part of the FOI internally financed project "*Deltagande i SoCTRix*" (which has been going on since January 2003 and has ended in December 2004) the following activities have been performed within the frame of the project:

- Participating in the SoCTRix demonstrator project (Jan. 2003 - April 2004).
- Presenting summaries both internally (FOI seminar - May 2004) as well as externally (FOI/FMV *Teknik-samordningsdagar* - May 2004).
- Participating in international conferences and symposiums (*International Software Radio Conference* - June 2003, *International Microwave Symposium* – June 2004, *European Microwave Week* – October 2004).

# 2. Flexible Radio Systems in Network Centric Warfare

This chapter deals with the use of more flexible communication systems, such as SDR, in network centric warfare. The main drive behind using a SDR concept is the simplicity of the radio system enabling technological and architectural advantages and thereby reduced size and cost. Reduced complexity is however associated with a possible loss of performance which might lead to a trade-off in terms of functionality versus flexibility. The SoCTRix project (see chapter 3) fits well into the development of SDR concepts both for civilian and military use. In the SoCTRix transceiver demonstrator, focus is on WLAN and 3G communication standards, but the incorporation of other communication methods or even sensor functions with adequate performance might be possible. The SoCTRix transceiver uses a direct conversion architecture supporting a number of different communication standards. This transceiver demonstrator aims at enabling technologies for future low cost and high integration multi-standard wireless wide band communication systems. This vision also touches the ambition of future network centric warfare where access to low cost multi-function communication systems is of crucial importance.

## 2.1 Software Defined Radio

The concept of SDR aims at the possibility to use only software or digital hardware to realize the radio functionality. This seems attractive since a lot of the size and cost consuming RF/analogue hardware then potentially could be omitted. Compared with more traditional radio systems, SDR gives rise to a new range of possibilities but is also associated with limitations. The NATO $C^3$-Agency [1] have identified some of these aspects as:

*Traditional Radio:*

- *Fixed number of systems, decided at initial design.*
- *Services can be multiple but decided at design.*
- *Reconfigurability possible but limited.*
- *Scalability not required.*
- *Limited up-gradability.*

*Software Radio (Ideally):*

- *Multiple variable radio systems supported, not necessarily decided at design time (Similarity for services).*
- *Adaptable to channel/propagation conditions ("i.e. "self-optimizing"; jamming, interference, multi-path)*
- *Scalability in software and hardware.*
- *Upgrade by user (not service professionals) – OTA updates & upgrades.*
- *"Future-proof"*

In [2] a multi-role multi-band radio demonstrator is described. It is developed by Thales and incorporates 9 different waveforms in the 0.6 – 1.5 GHz frequency range. Further examples of SDR implementations are from hand-held radios, mobile phones to communication terminals and can be found in [1], for example. A simplified (block level) schematic of a possible SDR architecture is shown in Fig. 1 [1].

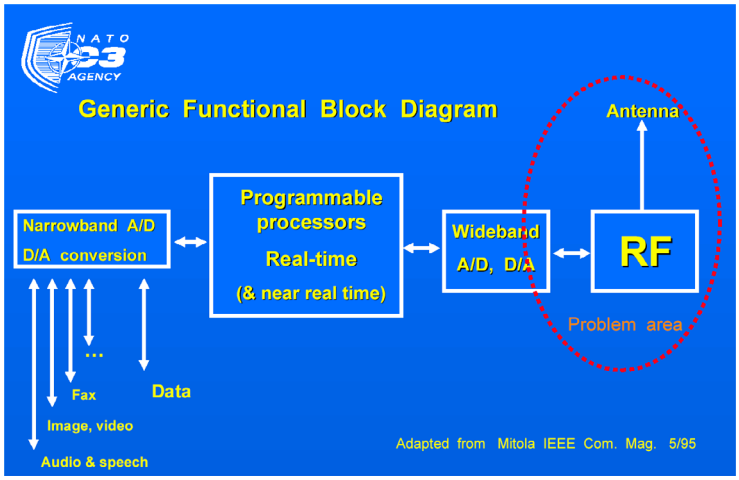


**Fig. 1.** Simplified (block level) schematic of an SDR architecture [1].

Advances and development of software defined radio systems and how well these can adapt to different needs of network centric warfare is an area where a lot of effort is still made and research is going on. In [2] a number of enabling technologies for SDR hardware are listed:

- High-speed, low latency busses.
- High-speed, low power processors.
- High-density memory.
- High-speed A/D converters.
- Efficient VHDL compilers.

### 2.1.1 Flexible RF architectures

In terms of minimizing the influence of a reduced RF-stage, the technological development on future high-speed A/D converters seems to be an important factor. Dynamic range, signal-to-noise ratio, bandwidth and operating frequency are all to a large extent decided by the A/D-converter number of bits, sampling frequency and maximum input power. Nevertheless, increasing demands for higher capacity (higher

data rates) communication networks (and in certain cases also with wide-range coverage) may result in more focus also being set on how to design the RF-part of the radio system. The NATO $C^3$-Agency has identified the RF and antenna parts as key areas that remain to be solved [10]. One key area is highly linear power generation for transmitting (i.e. high linearity power amplifiers). Other key areas are [1]:

*RF system:*

- *Dynamic range, extracting a signal at very low level.*
- *Transmit-receive isolation.*
- *Rejection of out-of-band noise, jamming and interference (i.e. filtering).*
- *Enough amplification for digitization.*
- *Wide bandwidth phase characteristics.*

*Antennas:*

- *Antenna element size.*
- *Bandwidth.*
- *Gain vs. directional characteristics.*
- *Co-siting of antennas.*

Many of the aspects mentioned above are crucial solely with the application of wireless communication in mind. When discussing other functions such as radar and electronic warfare together with high data rate communication these problems are likely to impose even more severe restrictions in terms of sensitivity, dynamic range and output power. The Defense Advanced Research Projects Agency (DARPA) has launched two different initiatives focusing on RF component performance enhancements achieved by using new materials, devices and architectural concepts [3]. The first of these two initiatives aims at the exploitation of Wide BandGap Semiconductor (WBGS) materials (such as SiC and GaN) and devices to improve the performance of future RF components by orders of magnitude. It is anticipated that such efforts in the future will lead to SiC and/or GaN Monolithic Microwave Integrated Circuit (MMIC) technology being a viable alternative for high power and high linearity applications in which bulky microwave power modules (based on vacuum electronics) are currently the only option. This will enable lighter, cheaper, and more efficient high discrimination sensors and communication transmitters.
The second DARPA initiative, referred to above [3], focuses on new component architectures in which digital and RF Micro-Electro-Mechanical System (MEMS) technologies are introduced into MMIC processes to achieve real-time optimization of the analog functions. The so-called Intelligent RF Front-End (IRFFE) initiative aims at demonstrating a new class of highly integrated RF and mixed-signal components that through self-assessment and optimization can adapt to rapid and unforeseeable changes in the environment or operational demands (see Fig. 2 below). This novel class of intelligent MMIC's aim at providing system designers with new degrees of freedom necessary to meet future network centric warfare requirements. Digital control or intelligence in the integrated circuit will be capable of optimizing the component architecture and performance at any given frequency within the operating bandwidth of the core active device(s). The IRFFE initiative envisions that a single component (or front-end) will be capable of meeting the performance requirements of various functions (such as communication and radar, for example) enabling multi-functional operation through a single aperture [3]. Such intelligent (or highly flexible)

micro-systems will have the ability to self-optimize in real-time their efficient-performance over broad bandwidth, overcoming the trade-offs that current analog components must endure. This unique ability is expected to lead to very efficient systems with reduced size, weight, power and cost. In order to demonstrate the concept of intelligent RF components, the following technical challenges must be addressed, according to [3]:

- Development of embedded analog sensors and algorithms for self-assessment and intelligent control of the analog performance.
- Demonstration of real-time adaptation through the implementation of RF MEMS technology to innovative MMIC designs.
- Demonstration of heterogeneous integration of mixed-signal technologies.

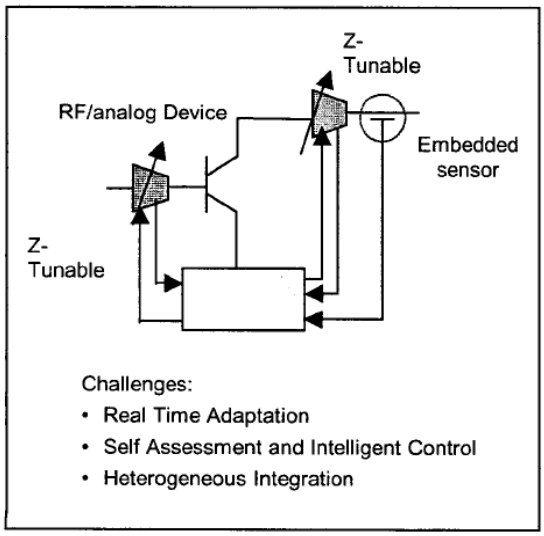


**Fig. 2**. Schematic description of an Intelligent RF Front-End (IRFFE) that should be able to reconfigure it self in order to adapt (in real time) to rapidly changing system needs and requirements [3].

It seems evident that even in the future, military forces will need different types of communication systems and equipment depending on different requirements on performance versus cost (i.e. commercially available components as well as others that are tailor-made for specific defense purposes) [4]. As described above, a lot of efforts are already going on in the U.S. (mainly financed by DARPA) in order to meet the demands of future military and commercial markets. In Europe, on the other hand, on going as well as future planned R&D efforts should aim at maintaining the independence and competitiveness of the European industries. To be able to achieve this objective, however, state-of-the-art component availability and independence from supply restrictions must be ensured. From a Swedish (as well as from a European) perspective further research on flexible RF architectures will be needed for several reasons. First of all, further research is needed in order to estimate the usefulness of this technique and its potential applications. Secondly, research could also provide access to the new capabilities and advantages that systems based on flexible RF architectures are expected to have in the future.

## 2.2 Network Centric Warfare and JTRS - A US Military Approach

JTRS (Joint Tactical Radio System) is a US military approach to standardize architecture and technology for a number of different systems to reach the goal of interoperability and flexibility (see Fig. 3). An important parameter is to use standardized waveforms.

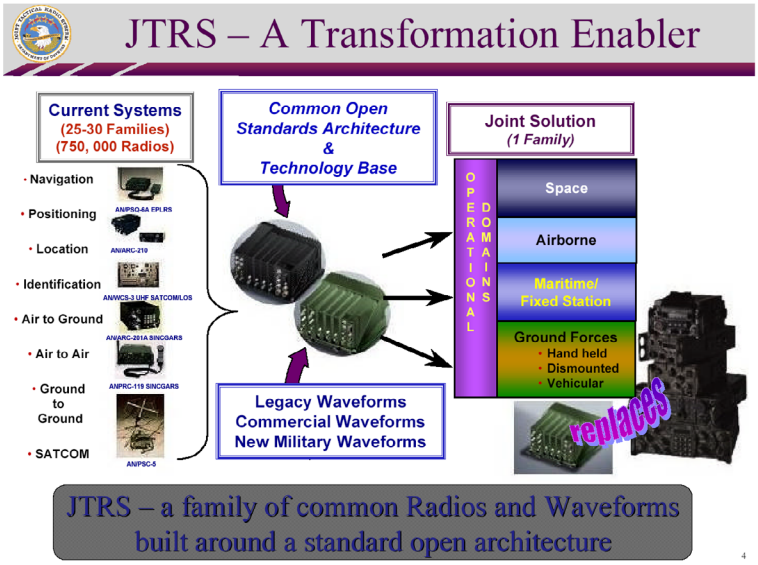


**Fig. 3.** An illustration of JTRS (Joint Tactical Radio Systems) [5].

The development of this idea is focused on a number of clusters representing different functionality and platforms (see Fig. 4) [5]. The clusters represent different army, naval and airborne based platforms together with communications, embedded and high data rate systems. They are all centred round the *Joint Software Communications Architecture* (JSCA) for sharing of information in a network through voice, video and data. The *Software Communications Architecture* (SCA) is the backbone. The ambition is to keep this architecture open and available to systems other than JTRS. The Swedish Armed Forces have chosen to adapt future military radio systems *Gemensamt Taktiskt Radio System* (GTRS) so that they should be SCA compliant and defined by JTRS [4]. More information on the development and structure of SCA can be found in [6-7].

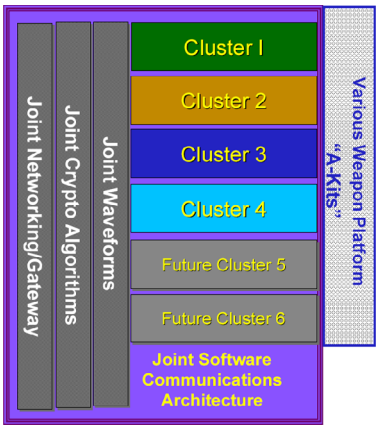


**Fig. 4.** Illustration of the JTRS development program supporting different clusters [5].

# 3. The SoCTRix Project

## 3.1 What is SoCTRix?

SoCTRix is a *multi-band and multi-standard radio transceiver demonstrator* research project, defined and run under the Swedish Socware program (see Fig. 5 for an illustration of the main concept of the SoCTRix project) [8]. The SoCTRix project (that started in April 2002 and ended in April 2004) serves as a common technical platform for the active cooperation between partners from national and international industry, universities and research institutes. The Swedish Defence Research Agency FOI joined the project in January 2003. The Swedish microelectronic research institute Acreo was responsible for the management and technical coordination of the project and also took the responsibility for the system design and development of the actual transceiver hardware and software. Altogether, nine industrial partners (Agilent, Samsung, Cadence, VIA Technologies, Bitsim, Catena, ARC, Chartered semiconductor, Jazz Semiconductor) together with seven universities (LiTH, LTH, KTH, CTH, MDH, Mid Sweden University, and NTNU) and three research institutes (FOI, Shanghai IC R&D and Acreo) have been involved in the SocTRix project. The project was originally defined to run over 2 plus 1 year (starting in April 2002) with a third optional year intended to target the final integration of the design blocks that were developed during the first two years. Due to discontinuing financial support the project was ended after two years in April 2004. A project model was used that allowed ideas and results from research at the universities and institutes to be evaluated, implemented and tested in a "real" test platform, aiming at a realistic application. Industry partners got good insight into and contact with current research as well as actual IP in return for their member fee. Further details on the technical scope and the main results achieved within the project can be found in [8].

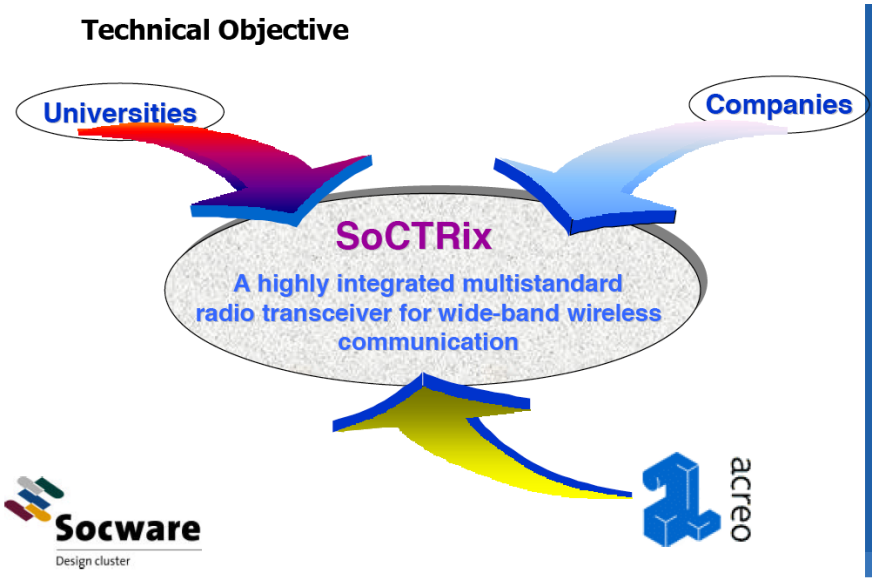


**Fig. 5.** Illustrating the main concept of the SoCTRix project [8].

### 3.1.1 Technical scope and project overview

The SoCTRix project targets development of technology enabling future 4G (*4th generation*) applications where there is a need for low cost flexible radio terminals capable of both 3G cellular and wireless LAN (*Local Area Network*) communication

(see Fig. 6). High data throughput is supported with local coverage by WLAN technology in the 2.4 and 5-6 GHz bands (*IEEE* 802.11a,b and g standards) and lower data throughput with wide coverage is supported through W-CDMA (*Wide-band Code Division Multiple Access*) in the 2GHz band. The ultimate goal of the SoCTRix project was to develop a highly integrated radio transceiver covering all of these standards and using technologies that are, or will be, available at a competitive cost level within a two or three years time horizon. This should be possible through the common resources and efforts of universities, institutes, and industry but also through the advantage of having control of and access to almost all domains of the design; radio architecture, analog, mixed signal, and digital circuit design, signal processing and algorithms; and package and substrate design.

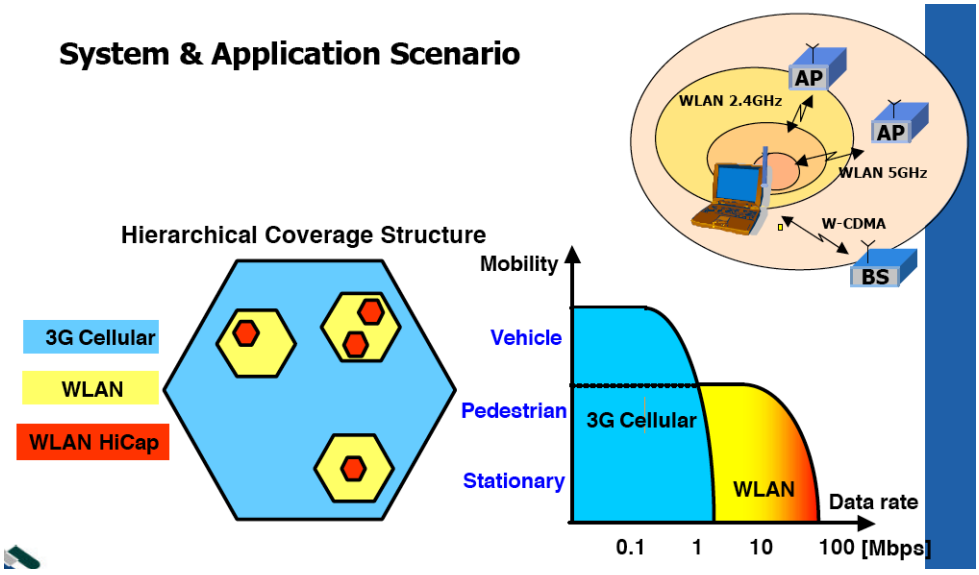


**Fig. 6.** Illustrating trade-off between data rate and mobility in 3G cellular and high capacity WLAN systems [8].

### 3.1.2 System design – technologies and physical partitioning

For several reasons, 0.18µm gate length CMOS (*Complementary Metal Oxide Semiconductor*) technology was selected as the preferred semiconductor process. One important factor that speaks in favour for choosing CMOS is based on the project ambition to keep as much of the system as possible on-chip, as low cost as possible, and provide high flexibility in the analog-digital system partitioning. At an early stage in the project there were clear indications that a complete system-on-chip (SoC) implementation would probably not be technically feasible within the given resource frame. One reason for this is the relatively low PAE (*Power Added Efficiency*) of linear CMOS power amplifiers (PA) something that in combination with the low supply voltage (1.8V nominally) makes it practically impossible to reach even close to the PA performance required. Other reasons are substrate noise coupling, thermal aspects and design flexibility, which combined make a hard case against a full SoC implementation. A System-on-Package (SoP) implementation, on the other hand, expands the available design space and offers the system designer possibilities to select optimal processes for different demands of the power, analogue and digital parts of the radio system. In addition, it naturally integrates the package and substrate as a resource for design and may actually result in a denser design compared with a

complete SoC solution. Figure 7 shows a schematic description of the physical partitioning of the SoCTRix transceiver based on a three-chip (mixed & digital, analogue and PA) SoP solution. Figure 8 shows a (six element) transmit/receive prototype antenna array that it intended to cover all frequency bands of the three different standards used in the SoCTRix transceiver demonstrator (i.e at 2, 2.4 and 5-6 GHz, respectively).

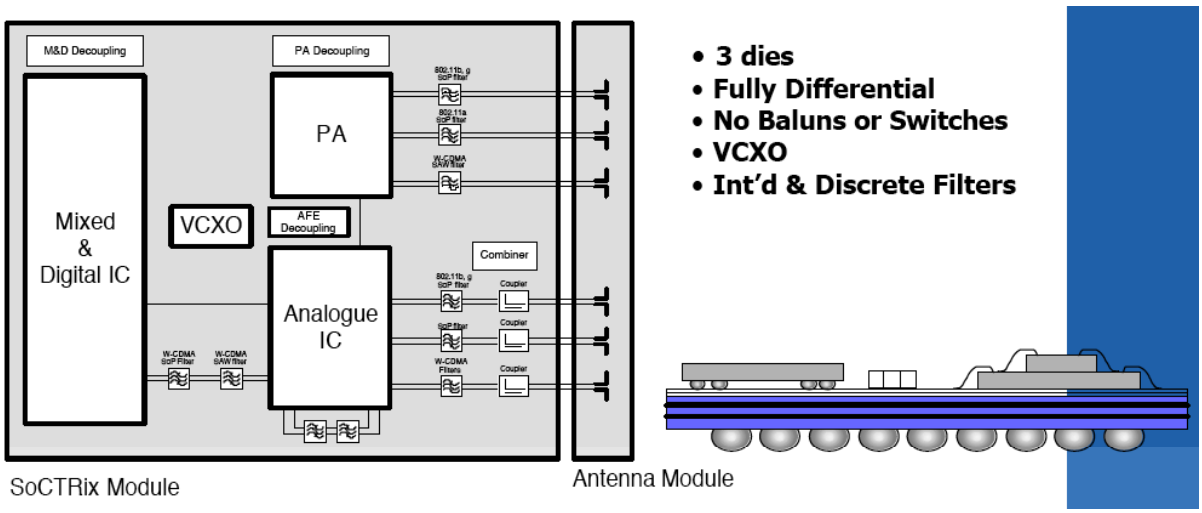


**Fig. 7.** Conceptual over-view of the physical partitioning of the SoCTRix transceiver [8].

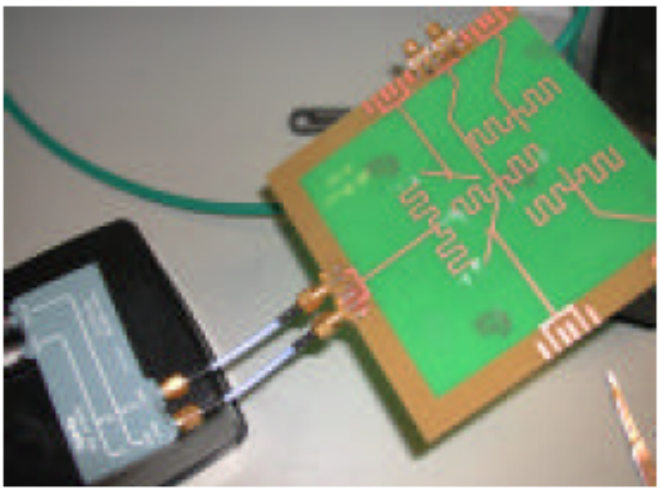

**Fig. 8.** Photo of a transmit/receive prototype array antenna for the SoCTRix transceiver [8].

## 3.2 Areas within the SoCTRix project where FOI has contributed

Next, we will describe, a bit more in focus, system areas and some key areas of circuit design within the SoCTRix project where FOI in a close collaboration with Acreo has contributed with research and development work. System studies of different radio standards supported in the SoCTRix transceiver are treated in section 3.2.1. The design and simulation results of a 5GHz active RF front-end filter implemented in a 0.18µm CMOS process are shortly described in section 3.2.2. Finally, in section 3.2.3, we summarize the design and results of a 5-6GHz SiGe BiCMOS PA.

### 3.1.1 System level studies

This section explains, a little bit further, the system design and some technology related aspects of the SoCTRix transceiver. FOI's involvement in the SoCTRiX project on system requirements and specifications has primarily been in relation with the transmitter system design for the 802.11b standard. The ultimate goal of the project is to build a highly integrated multi-standard and multi-band radio transceiver for wireless communication. Figure 9 shows a conceptual comparison between different radio system architectures that are based on a pure software defined radio (SDR) approach and on a stacked radio approach, respectively.

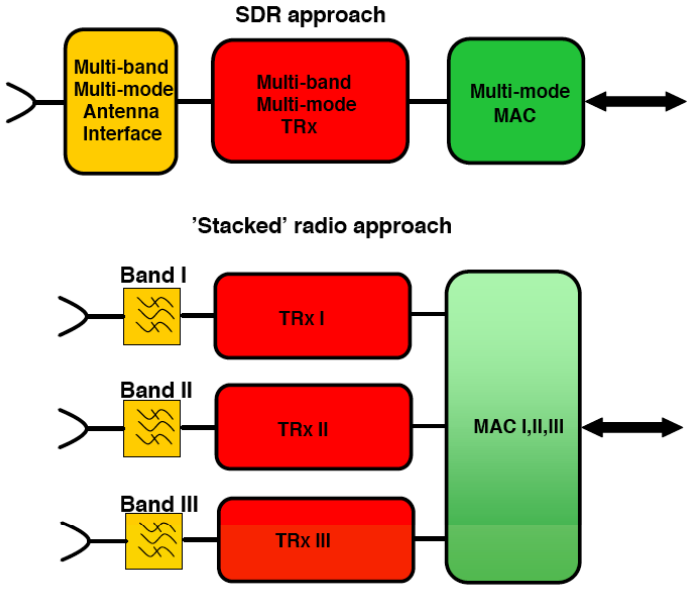


**Fig. 9.** Conceptual comparison between different radio system architectures that are based on a software defined radio (SDR) approach and on a stacked radio approach, respectively [8].

Instead of using of using separate solutions for each communication standard and connecting them in a stacked approach, in an SDR architecture common functions and functionality are assembled into multi-function modules. This includes all areas of the design; the radio architecture, analogue, mixed signal and digital circuit design, signal processing and algorithms, package and substrate design. The SoCTRix-project targets future 4G applications with low cost flexible radio terminals capable of both 3G and wireless LAN communication. High data throughput with local area coverage is supported by WLAN technology in the 2.4 and 5-6 GHz bands, while lower data throughput and wide area coverage is supported through W-CDMA at 2GHz. The different communication standards considered in SoCTRix are listed in Table 1.

**Table 1.** Summary of different communication standards used in the SoCTRix transceiver.

| Standard | Frequency [GHz] | MODEM |
|---|---|---|
| IEEE 802.11a | 5.1-5.8 | OFDM |
| IEEE 802.11b | 2.4-2.48 | CCK, DQPSK |
| IEEE 802.11g | 2.4-2.48 | OFDM |
| W-CDMA | 2 | - |

*System design over-view and some technology related aspects*

Figure 10 shows a schematic description of a target overall architecture for the SoCTRix transceiver. Since a complete SoC solution for the entire system was considered not practically feasible at this stage, a SoP solution was decided upon (see section 3.1). This means using a common substrate where different functions can be integrated directly on the substrate or by different mounting techniques. Since major parts of the system are digital, a 0.18 µm CMOS process was chosen as the primary candidate to be used for the integrated circuits. The high frequency characteristics of deep sub-micron CMOS also suggested that such a technology should be a viable alternative for most parts of the RF front-end. For the power amplifiers used in the RF front-end, however, a SiGe (*Silicon-Germanium*) HBT (*Hetero-junction Bipolar Transistor*) process technology was chosen due to the relatively low power added efficiency in the CMOS process. The project ambition of a high integration level resulted in the choice of a direct conversion architecture. This introduces design issues such as signal dependent DC-offset, quadrature imbalance, VCO pulling and LO-leakage that all have to be solved. The A/D-converter should have 8-10 bits and a sampling frequency of 40 MHz. The algorithm design is implemented in VHDL (*Very High-level Design Language*) and prototyped on FPGA (*Field Produced Gate Array*).

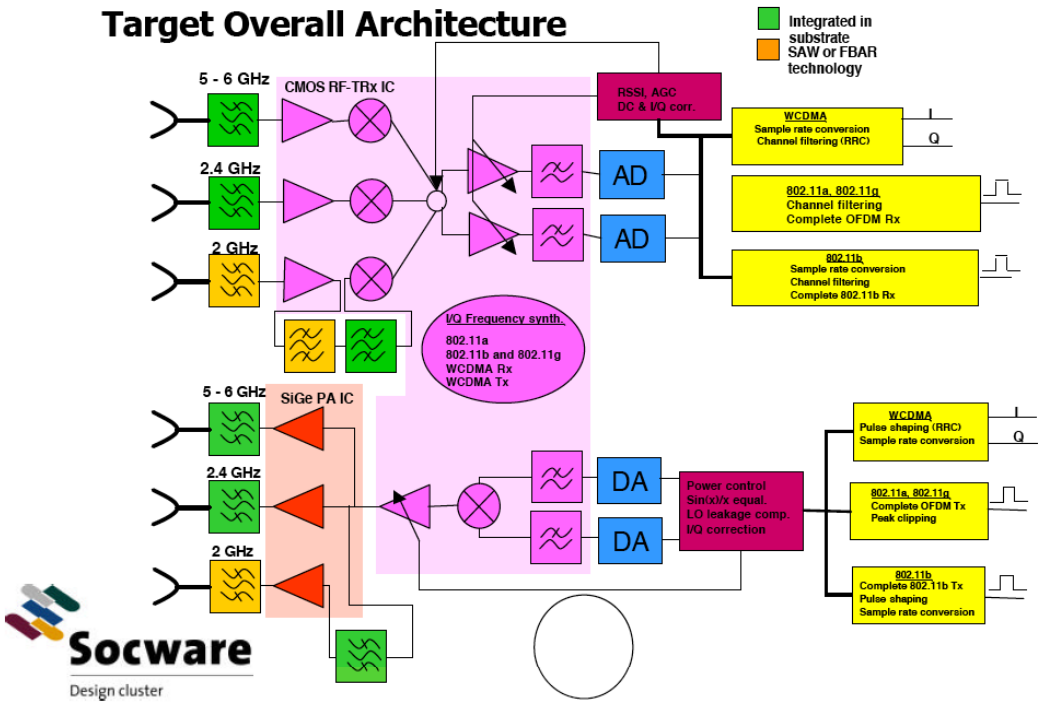


**Fig. 10.** Target overall architecture (block level schematic) for the SoCTRix transceiver [9].

*Transmitter system design (802.11b mode)*

This section describes, a little bit more in detail, the part of the SoCTRix system design where FOI have been directly involved which is in the transmitter system design for the 802.11b mode. Partitioning of the transmitter design requirements is carried out with the target of reaching a design compliant with the air-interface requirements given in [10]. The transmitter system design for 802.11b can be found in [9]. In Fig. 11, a block diagram overview of the transmitter is given to illustrate the level of abstraction in this design work.

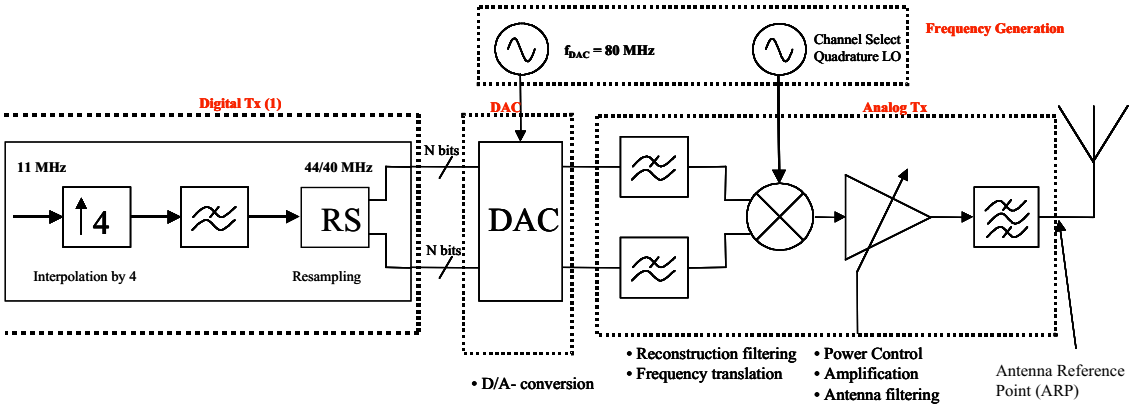


**Fig. 11**. SoCTRix 802.11b mode transmitter block diagram [9].

Basically, requirements are derived on the noise and distortion performance of each of the Digital Tx, DAC, Analog Tx and Frequency Generation blocks. To be able to complete the design a number of assumptions must however be made and they are stated below.

- The output from the DAC is assumed to be an analog complex baseband signal.
- The rate of the complex data entering the DAC is 40 or 80 MHz. If, at a later stage, digital predistortion is included in the SoCTRix solution, the rate must be increased significantly to accommodate the bandwidth expansion of the predistorted signal.
- Interpolation by two (2) or four (4) is used to reach the desired sample rate of 40 and 80 MHz, respectively. Interpolation (halfband) filter(s) is used to suppress the spectral images after upsampling.
- The phase noise is contributed by the DAC-clock and the local oscillator(s) used for frequency translation.
- Time domain windowing (instead of filtering) is applied, if required, in the transmitter to lower the spectral splatter (up to 10 MHz offset from center of band) of the transmitted signal.
- Analog lowpass reconstruction filters are used after the DACs.

Since the requirements on noise and distortion are dependent on the selectivity of the transmitter, it is also necessary to include requirements on the frequency response of the interpolation and reconstruction filters. Re-sampling is performed in the transmitter dependent on the rate of interpolation. Further assumptions that are necessary for the dimensioning of the transmitter are:

- Maximum output power level at ARP (Antenna Reference Point).
- EVM (Error Vector Magnitude) as a function of SINAD (SIgnal to Noise And Distortion ratio).
- Definition of DAC full-scale output power and reference point.
- I/Q DAC update frequency.
- Performance of digital transmitter in terms of transmit spectrum.
- Resampling.

The dimensioning is carried out for both in- and out-of-channel noise and distortion. Sources for noise and distortion that are identified and effect both or either of the in- and out-of-band rejections are:

- Local oscillator phase noise.
- Numerical noise generated in the digital Tx.
- DAC noise level.
- DAC and analog Tx IMD (InterModulation Distortion).
- Harmonic distortion in DAC and analog baseband components.
- Quadrature modulator gain/phase imbalance.
- Noise level of the analog Tx.

### 3.1.2 RF front-end studies: A 5GHz active filter in RF CMOS

*Background*

As a part of the SOCTRix-project, the RF performance of a silicon based active front-end filter was initially studied on a schematic circuit level in a pre-study [11]. Based on these initial results a layout implementation of such a filter was later derived within the FOI project *BFA* (*Radarsystem och Bredbandiga FlerfunktionssAntenner*) financed by *FMV* (*Försvarets MaterielVerk*). The active filter implementation was then fabricated in a 0.18μm RF CMOS process technology at the expense of the SOCTRix-project [12]. The interest for FOI to implement such an active filter is many-folded since this type of filter potentially could be used in various applications (not only in highly integrated radio transceivers but possibly also in the RF front-ends for radar and electronic warfare functions as well). Having said that, the main focus in our studies has been to evaluate the possibilities and the difficulties to implement the specific active filter design using an RF CMOS process of the type mentioned above. Below, we describe the main design ideas and methodology used in our filter implementation together with a summary of the typical RF performance achieved. The circuit schematic description of the filter together with all obtained results can be found in [12-13] and some results are also summarized below. The main objective in our approach has been to investigate possibilities to replace the LNA (Low Noise Amplifier) and passive off-chip RF front-end filter combination that are used in conventional transceivers with an active RF front-end filter instead. A reason for using an active filter in the RF front-end is that such a filter could be made highly integrated (on-chip) in contrast to a passive off-chip filter that often can be rather bulky and costly. The filter described in this report targets primarily the requirements for the IEEE 802.11a mode (i.e. it is intended to be used in the 5-6GHz frequency band). It should, however, in principle also be possible to use the same design methodology to realize the same type of active filter at 2.4GHz, for example. Such a filter could then potentially also be used in the RF front-end for the IEEE 802.11b and g standards as well. In this report, we focus our interest for this type of filter to multi-band and multi-standard transceivers, like the one developed within the SOCTRix project, for example. Studies of the possibilities and the limitations of using this type of filter in the RF front-ends of multi-function radar systems, on the other hand, can be found in [14]. The results of our proposed RF CMOS active filter design were also published and presented at the 2004 European Microwave Conference, held in Amsterdam, Netherlands, in October this year [15].

*General Description of Design*

A first order recursive active microwave filter may be realized by connecting an LNA and two couplers in a positive feedback arrangement. A high filter gain and out-of-band rejection is obtained when the gain in the feedback loop approaches one in magnitude if also the total feedback loop time delay is being equal to a multiple of $2\pi$ at the filter center frequency ($f_c$). The recursive active filter described in this report consists, on the other hand, of three amplifier stages; two common-gate (CG) stages and one common-drain (CD) stage, together with a passive LC delay network that are connected in order to realize a positive feedback loop (See [12]).

*Design Strategy*

The design methodology chosen was to start with the design of the filter open-loop gain (i.e. the three transistor stages used in the filter design without the passive LC

delay network used in the feedback loop being connected). The two CG-stages (one at the input and one at the output of circuit, respectively) are designed in order to achieve a 50Ω input and output impedance. The CD-stage is designed to compensate for the losses of the passive LC delay network. The passive LC delay network is designed in order to obtain the desired center frequency (in this case at 5.4GHz). Initially, circuit simulations were made on a schematic level using ideal passives in the delay and for DC biasing (as inductive RF chokes and for DC block and RF decoupling). The ideal passive components were later replaced with corresponding non-ideal passives based on foundry-models.

*Simulation Strategy*
Small signal and large signal simulations of the active filter have been made using Cadence RF spectre. Filter s-parameters, noise figure and stability measures have been simulated in the small signal analysis. Two-tone filter linearity in terms of the third order intercept point ($IP_3$) has been simulated using PSS (Periodic Steady State simulator) and PAC in RF spectre. Two closely separated input tones, located at 5.410GHz and 5.411GHz, respectively, were used in the $IP_3$-simulations. The simulated filter results described in this report are based on the layout implementation of the active filter and include the effects of extracted resistive and capacitive (but not inductive) parasitics in the circuit layout.

*Design For Test*
The filter circuit has been designed in order to enable RF measurements to be made on-chip using RF and DC probes. It is also possible to connect DC bias through the use of bond wires. To be able to control the biasing of the three different transistor stages used in the filter separately, each stage has been designed with a gate bias pad and a drain bias pad.

*Key Design Challenges*
Key design challenges of an active RF front-end filter implementation are summarized below:

- High gain and out-of-band rejection
- Large tuning range
- Adequate input and output impedance matching
- Unconditional stability
- Low noise figure
- High linearity
- Low power consumption

*Description of The Device Under Test (DUT)*
Figure 12 shows a chip photo of our fabricated RF CMOS active front-end filter (total circuit dimensions equal 1.1x1.1$mm^2$). The s-parameters of the tested filter structure were first measured with the DC-bias applied to the fabricated circuit using DC probes. However, a DC-biasing test fixture was made at FOI (see Fig. 13 below) and used for all tests performed [13]. RF Ground-Signal-Ground (GSG) probes were used in order to connect the instruments applicable for the specific tests performed to the 50Ω (single-ended) input and output pads used on-chip.

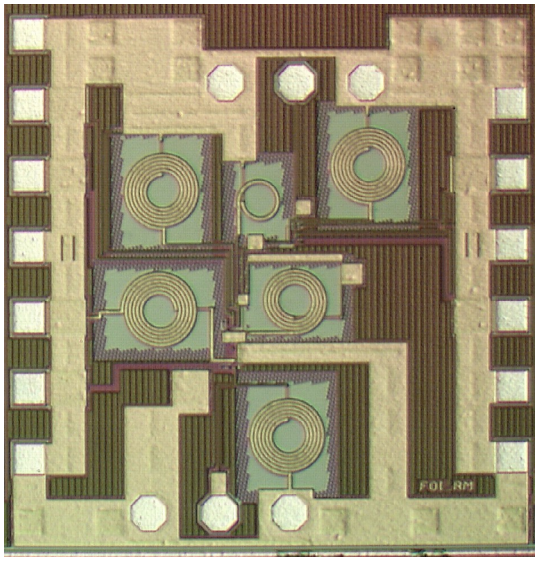

**Fig. 12.** Chip photo of a fabricated RF CMOS active front-end filter.

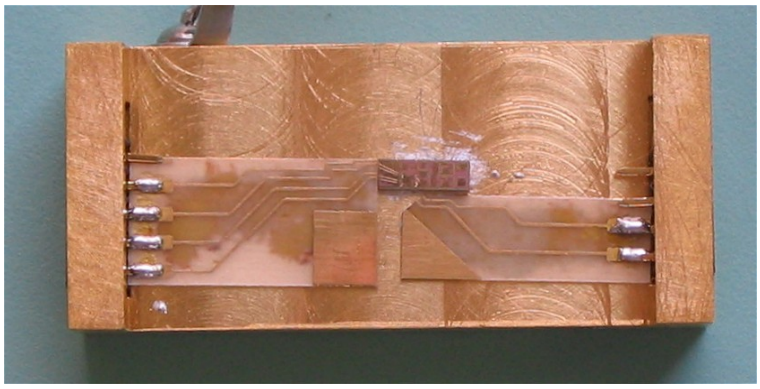

**Fig. 13.** A fabricated chip mounted on to a DC-biasing test fixture [13].

*Active Filter Results*

Below, we summarize the typical measured and simulated RF performance obtained for the active filter in terms of small signal gain, out-of-band rejection, noise figure and input referred $IP_3$ [13]. In order to be able to reach approximately the same DC current values as were obtained during simulation (i.e. $I_{DD1}$=5.94mA, $I_{DD2}$=10.14mA and $I_{DD3}$=8.27mA) the three transistor stages in the tested filter structure were first biased with $V_{DD1}$=$V_{DD2}$=$V_{DD3}$=1.8V and with roughly the same values of $V_{GG1}$, $V_{GG2}$ and $V_{GG3}$ as used in the simulation (i.e. around 0.8V, 0.8V and 0.9V, respectively). This resulted in measured values of the DC currents that were quite close to the expected results ($I_{DD1}$=5.95mA, $I_{DD2}$=10.18mA and $I_{DD3}$=8.25mA corresponding to a total DC power consumption of 43.9mW). Measured and simulated s-parameters of the DUT (when using the DC-biasing test fixture and this particular biasing) are shown in Fig. 14. The measured value of $s_{21}$ was in this case 6.8dB at the filter centre frequency, which is 2.5dB lower than simulated. A measured value of $s_{21}$ equal to 7.0dB was obtained when a $V_{DD}$ of 2V was used during measurement. The total current consumption was in this case marginally increased to 24.51mA as a result of the somewhat higher $V_{DD}$ used.

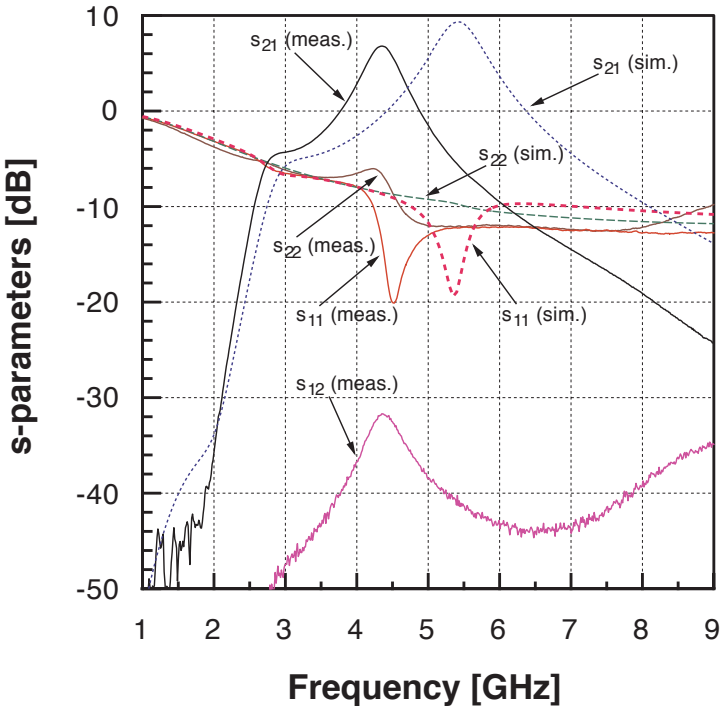


**Fig. 14.** Measured and simulated filter s-parameters [13].

Figure 14 further shows that an even larger deviation exists between the measured value and the simulated value of the filter centre frequency (4.4GHz measured compared with 5.4GHz simulated). It is believed that this discrepancy could be a result of several different factors that sum up together. The effects of process parameter variations on the filter small signal performance (in terms of deviation in filter gain and filter centre frequency) were briefly studied on a schematic level in the SoCTRix front-end pre-study [11]. In this study, a ±20% process parameter variation of the capacitor values used in the filter design was found to result in a ±6-8% deviation in the simulated values of the filter centre frequency (corresponding to a centre frequency shift of ±300-350MHz). An even larger centre frequency shift could be anticipated if we also take into account the effects of process parameter variations in other types of components (such as transistors and resistors, for example). The type of nmos transistor we have used in the filter design together with the fact that the effects of parasitic inductance in metal wires were not taken into account during simulation are two other possible factors that partly may explain the relatively large difference found between the measured and the simulated centre frequency value. In simulations on a schematic circuit level, we obtain a centre frequency value that is 250MHz lower when the RF nmos transistors used in our filter design are replaced with digital nmos transistors. Finally, by roughly estimating the parasitic inductance values in different metal wires used in the filter design we have simulated (also on a schematic level) the effect of these parasitic inductances on the filter centre frequency value. The results indicate that a 150MHz lower centre frequency value could be anticipated if parasitic inductance is taken into account. Taking into account all the possible effects mentioned above (i.e. process parameter variations, type of nmos transistor used and parasitic inductance) we end up with a centre frequency value for the filter that may be (at least) 700-750MHz lower than what was simulated based on the final layout of our filter design. The typical measured and simulated filter results obtained are finally summarized in Table 2.

**Table 2.** Summary of active filter results [13].

| Parameter | Conditions | Req. | Sim. | Meas. | Unit | Comments |
|---|---|---|---|---|---|---|
| Transmission gain | @ $f_c$ | ≥10 | 9.3 | 7.0 | dB | Not OK (-3dB below target) |
| Noise Figure | @ $f_c$ | ≤10 | 4.7 | 5.9 | dB | OK (4dB below target) |
| Input referred 1dB compression point | @ $f_c$ | N/A | N/A | -6 | dBm | |
| Input referred third order intercept point | @ $f_c$ | ≥-6 | 3.5 | 2 | dBm | OK (8dB above target) |
| Out-of-band rejection | @ 2000 MHz | ≥45 | 43 | 42 | dB | Not OK (-3dB below target) |
| | @ 3600 MHz | ≥15 | 13 | 8 | dB | Not OK (-5dB below target) |
| | @ 8333 MHz | ≥20 | 20 | 27 | dB | OK (7dB above target) |
| | @ 4286 MHz | ≥5 | 10 | 0 | dB | Not OK (-5dB below target) |
| | @ 4667 MHz | ≥0 | 7 | 3 | dB | OK (3dB above target) |
| Power consumption | | | 44 | 44 | mW | |

*Summary and conclusion*

An active RF front-end filter has been designed, processed and measured. The simulated performance of the active filter has been verified against measurements showing on one side, a relatively large difference in centre frequency, but on the other side not too large discrepancies between measured and simulated values of gain, noise figure, $IP_3$ and out-of-band rejection, respectively. The measured centre frequency of the filter was found to be 1GHz lower than expected (4.4GHz measured compared with 5.4GHz simulated). Simulations imply that this discrepancy to a large extent possibly could be explained by several factors such as process parameter variations, parasitic inductance in metal wires and the accuracy of the transistor model used in the circuit design. The measured centre frequency gain was about 2dB lower than simulated. The measured noise figure and input referred $IP_3$ were about 1dB higher and 1.5dB lower than simulated, respectively, at the centre frequency. The maximum measured filter gain was 7dB, which is 3dB from target. The measured noise figure and $IIP_3$ are, on the other hand, 4dB and 8dB above target, respectively. The measured out-of-band rejection equals 42dB at 2GHz, which is close to the corresponding simulated value of 43dB and is also close to the target value of 45dB. To be able to fulfil the requirements for the IEEE 802.11a mode, the centre frequency of the filter needs, of course, also to be situated in the 5-6GHz frequency band. Filter gain should be improved by several dB's if the more conventional LNA and passive filter combination used in the SoCTRix transceiver should be replaced with an active RF front-end filter. It should also be more easily to fulfil the requirements for the IEEE 802.11b mode assuming that the filter is re-designed to operate in the 2.40-2.48GHz frequency band. The filter should also be made frequency tuneable in order to compensate for filter gain and centre frequency deviations due to process parameter variations or temperature drift. One possible way in which this could be achieved is to use, for example, a varactor-tuned delay circuit in the filter feedback loop. This has to some extent already been investigated on a schematic level of the filter circuit [11]. Finally, in order to make the active filter design fully compatible with the SoCTRix transceiver, a differential active filter implementation should be investigated.

### 3.1.3 RF front-end studies: A 5-6GHz SiGe BiCMOS power amplifier

*Purpose of the PA Design*

The SOCTRIX multi-standard transceiver demonstrator project targets a transceiver covering the standards 802.11a, 802.11b, 802.11g, and mobile W-CDMA. An initial PA design, served as the first step in the exploratory task of finding a sensible PA architecture, to meet the demands needed for the transceiver. In the first design of a PA in the SOCTRIX project, information concerning problems and pitfalls as well as process capabilities regarding high frequency and high output power was gathered for reuse. The first PA was selected to be designed for the IEEE 802.11a standard which covers the frequency range of 5.1 - 5.85 GHz. First a pre-study [16] was performed in order to foresee the possible forthcoming challenges and solutions. In the pre-study, only a single stage power amplifier was simulated. The output related 1 dB compression point was at 27 dBm with a power gain of 2 dB. Below, we summarize the evaluation of a three-stage PA designed using a SiGe BiCMOS process. Further results of this PA, described a bit more in detail, can be found in [17-18].

*Process Technology*

The simulation tool used was Cadence 5. 0. 0. The technology adopted for the PA is a SiGe BiCMOS process with an emitter width of 0.18 μm [17]. The process utilizes four levels of metal and deep trench npn devices. The transistor type used typically has a maximum $f_T$ value around 35 GHz while $f_{max}$ is 60 GHz. The collector to emitter breakdown voltage is 6 V. The current gain (beta) is 110.

*General Description of Design*

The Power Amplifier (PA_SiGe_1) designed is one of the three PA's needed in the SOCTRix project. This particular amplifier consists of a high power differential three-stage amplifier situated directly after the VGA in the transmitter chain and adopted for the 802.11a mode (Frequency band 5.1 – 5.85 GHz). It has the simple purpose of amplifying signal before radiating the information in the air. The PA consists of five main parts: *input matching circuitry* (PA_inmatch1), *pre-amplifier stage* (PA_pre_amp), *medium power amplifier stage* (PA_mid_amp1), *high power amplifier stage* (PA_power_amp) and *output matching circuitry* (PA_outmatch1). The PA_inmatch1 is needed to match the PA_pre_amp input impedance to a differentially input impedance of the PA of 100 Ω and the impedance transformation ratio is 2:1. The PA_pre_amp, PA_mid_amp and PA_power_amp stages amplify the signal. The PA_outmatch1 matches the output of the PA_power_amp for "maximum" output power and has a differentially output impedance of 100 Ω and an impedance transformation ration of 1:10. Since a high linearity of the PA is on the top priority (together with a reasonable output power level) the operating class was selected to be of type Class A (as it is being highly linear in theory).

*Design and Simulation Strategy*

The design methodology selected was to start with the last stage, the PA_power_amp, which is the "bottle neck" for the overall linearity. Moving backwards then in the amplifier chain the input matching circuit (PA_inmatch_1) was the last PA sub-circuit to be designed. The different blocks were then re-tuned iteratively in order to achieve optimal performance. The linearity was evaluated using a two-tone test with tones 10MHz apart and located in the middle of the frequency band at 5.5 GHz and 5.51 GHz. For the linearity simulations, Spectre RF PSS (single tone) and QPSS (dual

tones) have been utilized. S-parameters, DC and small signal AC simulations where also performed. Biasing information can be read out from the test-benches used. Note that the simulated DC values in the test-benches are at schematic level. To evaluate the different stages in more detail, all the biasing and supply pins are unique for each stage. Furthermore the output matching was designed for a 100Ω differential output resistance instead of 50Ω as specified in the Design Rule Specification. This, of course, sets even higher demands on the matching network. Three off-chip control resistors are used to set the current limits on the voltage bias generating instruments and they also assure temperature stability.

*Summary of Power Amplifier Simulation Results*

The PA_SiGe_1 has been simulated through process variations, different voltage settings and temperatures [17]. The input and output ports are set to 100 Ω. The linearity of the circuit is simulated using a two-tone test (RF Spectra QPSS). According to [9], the linearity is specified in terms of a third order intermodulation rejection ratio $IMR_3$ below -48dBc at 19dBm of output power. The simulated $IMR_3$ was –36 dBc and the gain varied from 22 dB and 25 dB, close to the target of 24 dB. Temperature and process variations where also simulated with little impact on the results. From the design specifications, the output related 1dB compression point (OP1dB) was defined at +25 dBm and the gain should be 24 dB at 5.5 GHz given a supply voltage of 3.3 V. Figure 15 shows the simulation results at different supply voltages. OP1dB varies between 24.1 and 23.4 dBm. The gain varies within 0.8 dB. The targeted power added efficiency (PAE) was 10% at $P_{out}$=19 dBm. This value seems to be difficult to achieve in a standard silicon germanium process of the type that we have been using here. Given an output level of 19 dBm, a PAE of 3.2% has been simulated. According to the [9], the input and output of the PA_SiGe_1 should be close to 100 Ω (differentially) at 5.5 GHz. A relatively good impedance match is achieved at the input port. The output port is however rather mismatched at 5.5 GHz.

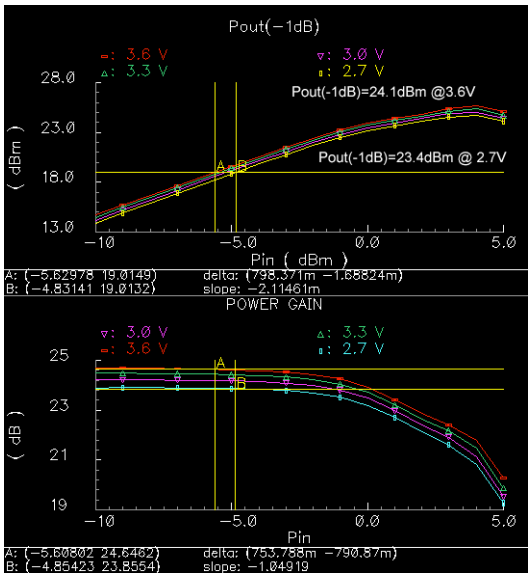


**Fig. 15.** Simulated PA output power [17].

Stability simulation was done using small signal analysis and the PA_SiGe_1 was found to be unconditional stable in the simulations.

*PA_power_amp (3rd stage)*
The PA_power_amp block is the final amplifier stage used in the PA chain. It sets the linearity for the complete PA. It has a power gain of 4.3 dB for a 10 Ω load and is biased by its input (i.e. PA_mid_amp1 output). Due to the high linearity demands, the last stage was chosen to be a common emitter with inductive emitter de-generation, working as a negative feedback. This is done in order to sacrifice gain for linearity and improve matching possibilities by raising the input impedance. Additional feedback was provided by the collector-base RC feedback link. Approximately 5% of the output current is utilized in feedback to the input. The base inductors have the same value as the degeneration inductors and provide stability for the PA_power_amp stage. Simulation of the PA_power_amp was done to characterize its influence of the PA_SiGe_1. The port impedances are set to resemble the source (PA_mid_amp1) and load (PA_outmatch1) impedance. Unfortunately, the Cadence software tool used only allows input and output ports to be set to real impedance values. This results in an uncertainty in the exact input power level axis of the simulation, but the gain is measured in the circuit and presented correctly. At 5.5 GHz, the power gain is 4.3 dB, which is due to a voltage gain of 1.2 and a current gain of 2.2. The input power level was selected to reach the overall output target level of 19dBm. The OP1dB is 23.3dBm. A rather poor PAE is achieved, mainly due to the high linearity demand.

*PA_mid_Amp1 (2nd stage)*
The PA_mid_amp1 block is the second active block after the PA_inmatch1 block. Its purpose is to forward a medium voltage signal and current drive the PA_power_amp block. This block also provides the biasing for the PA_power_amp. The PA_mid_amp1 works as a buffer with emitter followers and as a temperature stability circuitry for PA_power_amp. It is biased by a current source with an impedance boosting inductor at its output. Power gain is around 10.9 dB. Simulation of the PA_mid_amp1 was done to characterize its influence of the PA_SiGe_1. The port impedances were set to resemble the source (PA_pre_amp) and load (PA_power_amp) impedances. The absolute value of the source and load impedances at 5.5GHz is chosen, as 105 Ω for source and 18 Ω for load. At 5.5GHz the power gain is 10.8dB, which is due to a voltage gain of 0.9 and a current gain of 5. The linearity is relatively high, with an OP1dB above 15dBm. A rather poor PAE is achieved due to the high linearity demand.

*PA_Pre_Amp1 (1st stage)*
The PA_pre_amp block is the first active block after the PA_inmatch1 block. Its purpose is to amplify a rather small signal for the PA_mid_amp1 block. The PA_pre_amp is a differential amplifier, current biased by a common emitter current source with impedance boosting, inductive degenerated and using LC tanks at the outputs. Power gain is around 9dB. Simulation of the PA_pre_amp was done to characterize its influence of the PA_SiGe_1. The absolute value of the source and load at 5.5GHz is selected to be 48 Ω and 100 Ω respectively. At 5.5GHz the power gain is 9.5dB, which is due to a voltage gain of 3 and a current gain of 2.5. The linearity is relatively high (OP1dB is more than 10dBm). A rather poor PAE is achieved due to the high linearity demand.

*Output Matching Network*
The output matching is an implementation of a first order high pass filter. It is designed to have a differential 10Ω input and a 100Ω output, between 5-6 GHz. It

was optimized at 5.5 GHz to maintain a 10Ω impedance at the input. The output matching is between the output of the PA_power_amp and the probing pads. The schematic of the PA_outmatch1 circuit is shown in Fig. 16. The matching was done on the same chip as the other circuitry.

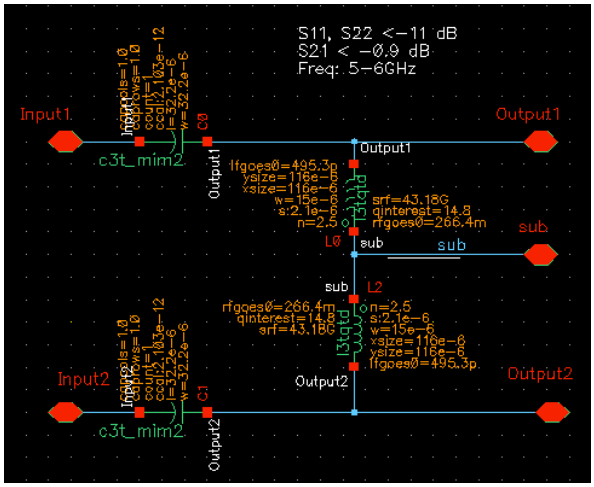


**Fig. 16.** Schematic of PA output matching circuit [17].

*Input Matching Network*

The PA input matching network is done in the same way as the output matching network. It is designed to have a (differential) 100Ω input impedance and a 48Ω output impedance between 5-6 GHz, optimized at 5.5 GHz. The filter is placed between the probing pads on the silicon die and the PA_pre_amp stage. The schematic of the PA_inmatch1 circuit is shown in Fig. 17. Small signal simulation over process variations shows that the insertion loss at 5.5GHz is maximum 0.5dB.

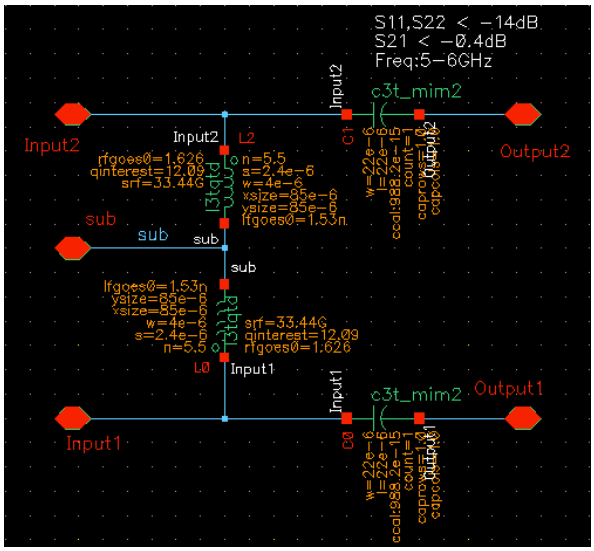


**Fig.17.** Schematic of PA_input matching circuit [17].

*Power Amplifier Measurement Results*

To be able to experimentally evaluate the fabricated PA design (first design iteration), a PA chip was mounted on to a PCB board and connected via bond wires to the DC

pads used on-chip. The Pre_Amp1 stage was tested and run to its maximum collector current. The mid amplifier was also independently tested and run to its maximum current level. In principle according to the design, the pre-ampl and mid_ampl are DC isolated. It was, however, found that when mid-ampl was biased and reached about 70% of its maximum current level, the collector current in the pre_ampl started to reduce by about 30%. Since in the design, the third power amplifier stage can only be run via the mid_amplifier, it was not possible to reach the maximum PA current level. There were also problems with oscillations in the third stage. The PA was later re-designed, so that each amplifier stage can be separately biased.

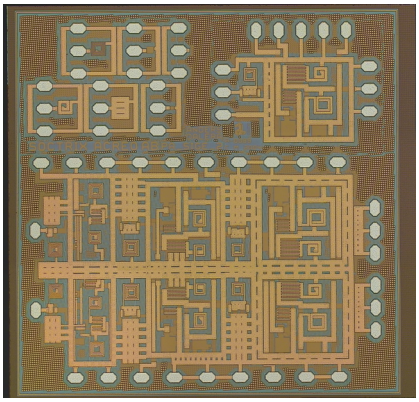

**Fig. 18.** Chip photo showing a SiGe BiCMOS PA developed within the SoCTrix project.

*Summary and Conclusion*

Research and development work has been focused on the design and evaluation of a balanced PA for the SOCTRix multi standard transceiver [17-18]. In simulations of a first PA design implementation, all parts of the PA target specifications were not reached [17]. Parameters that closely matched were simulated power gain (23dB, 24dB target), power flatness (2.5dB, 3dB target). Parameters that were not closely matched were linearity ($IMR_3$=-35dBc, -48dBc target) and PAE (3.2%, 10% target). Measured PA results were later obtained after a second design iteration [18]. A chip photo of a 5-6GHz SiGe BiCMOS PA (second design iteration) developed within the SoCTrix project is shown in Fig. 18. The measured results did not meet the given PA target specification and were also not obtained in accordance with simulations. Separate DC biasing of all three active stages were used in the second PA design. This resulted in much better control of the circuit. A large part of the PA inter-stage matching circuitry was also re-designed. At 5.5GHz (assuming a simulated input power per tone of –2.25dBm) the output power levels of the fundamental tones should (according to simulations) be equal to 16dBm and the $IMR_3$ should be at -32dBc. According to the PA measurements, however, they are equal to 6dBm and -36dBc, respectively (see Fig. 19). For a two-tone test with roughly -40dBc of IMR, the error vector magnitude (EVM) is between 3-3.4%. This corresponds to a backoff of 6-8dB from the OP1dB. Measurements on break out circuits that contain some typical passive components (on-chip inductors and capacitors) used in the PA show relatively large deviations compared with simulated values [18]. For example, the measured capacitance value (4pF) of an on-chip capacitor is equal to twice its simulated value (2pF). Even though the inductors used are found to be somewhat better modelled (than the capacitors) inaccurate modelling of the passives could be a possible error source that could explain the much lower measured output power level of the PA (6dBm compared with 16dBm simulated). The accuracy of the active device models

used is another question mark. The PA input matching achieved on PCB is fairly good between 4.8-6.5GHz. However, additional PA measurements should be done in order to be able to determine whether the input impedance match is a possible error source or not. The output impedance matching performs relatively well between 3.8GHz and 6.2GHz. The insertion loss of the output matching network used is typically 0.75dB.

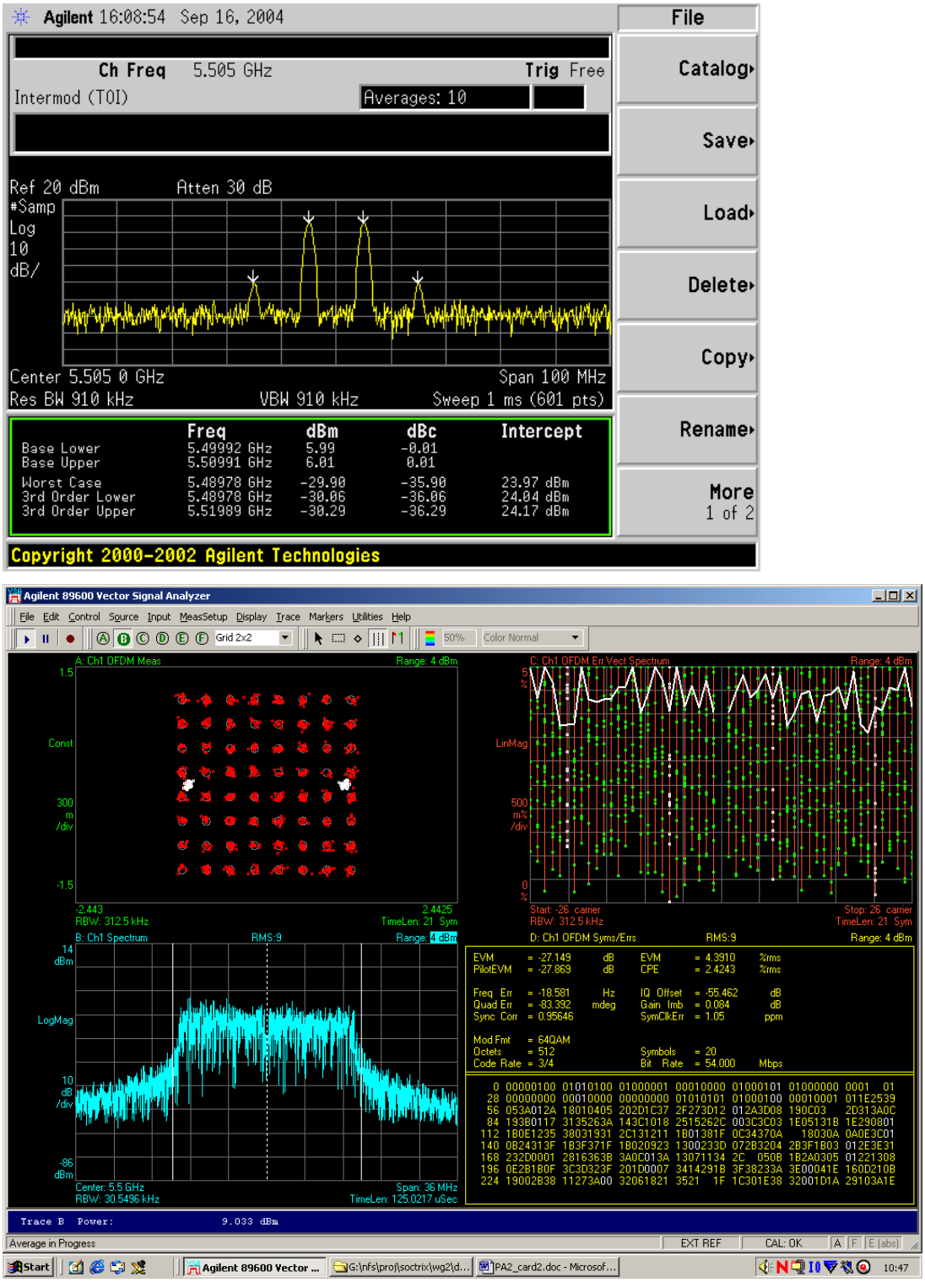


**Fig. 19.** Measured RF performance of a SoCTRix 5-6GHz SiGe BiCMOS PA [18].

## 3.3 Summary of results and conclusions from the SoCTRix project

Global trends in wireless communication are the need for higher data rates and the demands for seamless integration between different standards and these two features should be achieved at a reasonable cost. To be able to meet these requirements, new radio architectures will be needed that allow highly integrated low cost multi-standard and multi-band transceivers to be developed for the mass consumer market. Figure 20 depicts the multi-standard and multi-band transceiver architecture (on a component block level) that has been proposed and utilized within the SoCTRix project [8]. The proposed architecture should be capable of handling both 3G cellular telephony (W-CDMA) as well as WLAN (*IEEE* 802.11a,b and g standards) located at 2GHz, 2.4GHz and 5-6GHz, respectively, and with different requirements on coverage and data rate. To be able to fulfil this in a cost-efficient way, a design approach has been followed that utilizes a direct conversion architecture with an highly integrated fully balanced antenna front-end realized using low cost standard silicon technology.

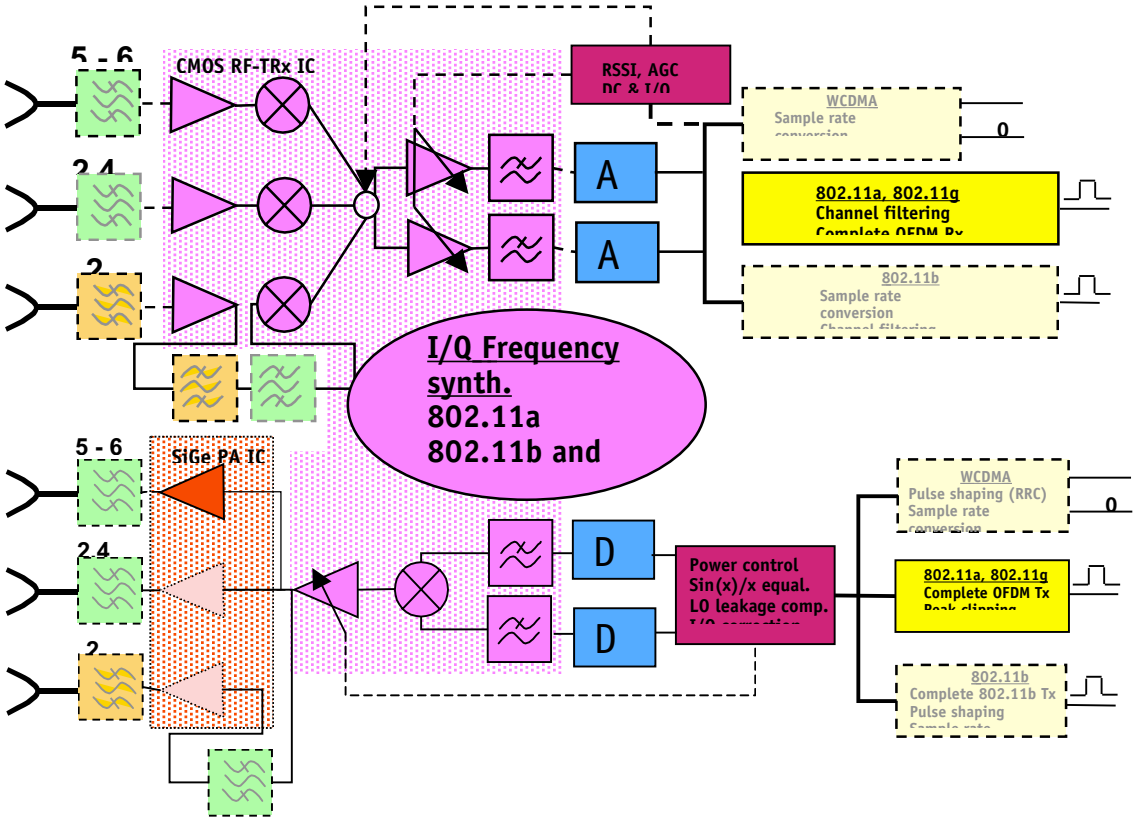


**Fig. 20.** Multi-band and multi-standard architecture proposed within the SoCTRix project [8].

By the time of the ending of the SoCTRix project (in April 2004) a good part of the different analogue and digital blocks that originally were intended to be used in the complete SoCTRix transceiver have been designed using a 0.18μm CMOS process. A 5-6GHz PA (intended for IEEE 802.11a) has been designed in a SiGe BiCMOS process technology (see section 3.2.3). Most circuit blocks required for a transceiver module supporting the standards of IEEE 802.11a,b and g (and also some parts supporting W-CDMA) have been designed and tested by the project ending (see Table 3 for a summary). Next, we present in a summarized way the main results achieved for some of the most fundamental parts of the SoCTRix transceiver. For the more interested reader, further details can be found in [8], for example.

**Table 3.** Summary of the main different parts of the SoCTRix transceiver [8].

| Transceiver part | Comments |
|---|---|
| RF front-end (WLAN 802.11a,b,g) | Designed and tested |
| RF front-end (W-CDMA) | Partly designed and tested (sub-parts only) |
| Power amplifier (WLAN 802.11a) | Designed and tested |
| Power amplifiers (WLAN 802.11b,g & W-CDMA) | Not designed |
| ADC & DAC | Designed and tested |
| Digital baseband | Designed and tested |

Figure 21 shows a chip photo of a WLAN 802.11a,b and g CMOS transceiver developed within the SoCTRix project (the chip area used is close to 4mm$^2$) [8]. The transceiver draws less than 100mW of DC power. The transceiver functionality has been tested both in the receive mode as well as in the transmit mode. The total variable gain range is close to 50dB in receive. For the 802.11g standard (i.e. at 2.4GHz), EVM is typically around 6-8%. EVM is mainly limited by phase noise at high input levels and by Rx noise figure at low input levels. Figure 22 shows the output power spectrum at 2.4GHz for a date rate of 54Mbit/s.

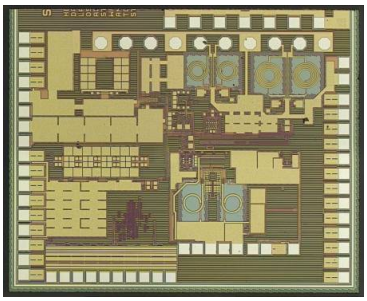

**Fig. 21.** Chip photo of an 802.11a/b/g transceiver developed within the SoCTRix project [8].

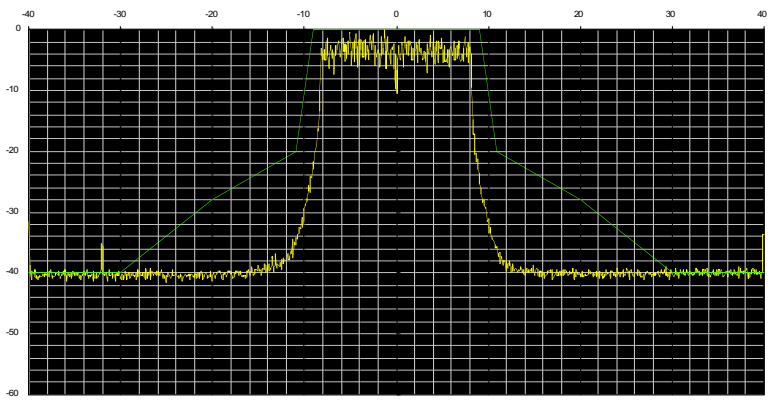


**Fig. 22.** Output power spectrum at 2.4GHz for 54Mbit/s (spectrum mask 802.11g) [8].

Figure 23 shows a chip photo a 10 bit ADC (with a 40MHz sampling frequency) that has been developed and tested within the project [8]. This ADC draws 36mW of DC power and has a spurious-free dynamic range (SFDR) of 69dB. A 10 bit ADC with higher sampling frequency (80MHz) but also higher power consumption (<150mW) and lower SDFR (around 60dB) was designed at the end of the project [8].

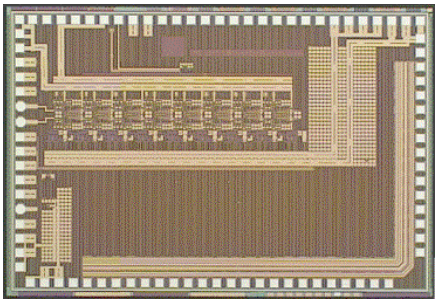

**Fig. 23.** Chip photo of a 10 bit 40MHz ADC developed within the SoCTRix project [8].

Figure 24, finally, shows a chip photo of an 802.11a/g baseband circuit (OFDM modem Tx path, see Fig. 20 above) that also has been developed and tested within the project [8]. Operating frequencies are equal to 20MHz and 40MHz, respectively. The total chip area used is 2.5x2.5mm$^2$.

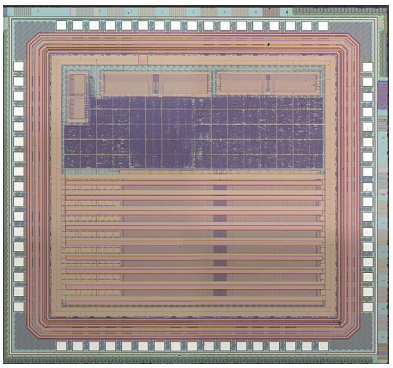

**Fig. 24.** Chip photo of an 802.11a/g baseband circuit (OFDM Modem Tx path) developed within the SoCTRix project [8].

In summary, the main results and conclusions derived from the SoCTRix transceiver project can be described as follows [8 and 19]:

- A System-in-a-Package (SoP) hardware solution, rather than a complete System-on-a-chip (SoC) solution, was adopted for the targeting applications.
- The use of low cost technologies enables compact and inexpensive system solutions.
- Limited possibilities of re-use of different analog and digital sub-system parts.
- Most functions implemented in analog hardware and not in digital software.
- System integration and WLAN development proceeded ahead of plans.
- W-CDMA and SoP design did not reach as far as was originally planned.

# 4. Conclusion

In this report, we have presented an overview of possibilities and challenges that exist when trying to realize systems for more flexible communication (such as e.g. software defined radio and multi-band multi-standard wireless communication). The use of multi-band and multi-standard wireless communication could be advantageous in order to increase the possibilities to circumvent hostile jamming and may also facilitate interoperability at international operations, for example. The idea of using more flexible radio systems seems to be particularly attractive in such cases when certain missions should be accomplished that can be difficult to foresee (and thus plan for) in advance (for example, during peace-keeping or peace-enforcing operations). However, trying to combine different standards and frequency bands can be expected to result in challenges related to issues on a system architecture level as well as when it comes to the actual hardware implementation on a sub-system level. Already today and also in the nearest future, armed forces will need different types of communication systems and equipment depending on different requirements on performance versus cost (i.e. commercially available components as well as others that are more advanced and tailor-made for specific defense purposes).

To increase knowledge and competence related to methodology and technology for multi-band and multi-standard wireless communication in future network centric warfare, FOI Sensor Technology has participated in a research and development project called “SoCTRix”. The primary goal of the project has been to demonstrate possibilities to realize a highly integrated and low cost radio transceiver suitable for multi-standard and multi-band wireless communication. One important conclusion made is that the type of multi-standard and multi-band RF architecture proposed and utilized within the SoCTRix project does not fully solve the task of implementing truly flexible RF communications systems. A reason for this is due to the limited possibilities of re-use of different analog and digital sub-system parts of the RF transceiver. Most functions have in this case been implemented in (analog) hardware and not in (digital) software. Thus, radically new RF architectures and components will be needed to be able to realize RF communications systems in the future that are drastically more flexible than today’s systems. Tuneable RF front-end amplifiers and filters are examples of key components that could enable more flexible architectures. A 5GHz tuneable active filter (or band pass amplifier) is an example of such types of components that has been investigated in the project (using a low cost technology) and with some promising results achieved.

A lot of activities are also going on mainly in the US in order to meet the demands of future military and commercial markets regarding more flexible RF architectures and components. In Europe, on the other hand, on going as well as future planned R&D efforts should aim at maintaining the independence and competitiveness of the European industries. To be able to achieve this objective, however, state-of-the-art component availability and independence from supply restrictions must be ensured. From a Swedish (as well as from a European) perspective, further research on flexible RF architectures and components will be needed for several reasons. First of all, further research is needed in order to estimate the usefulness of this technique and its potential applications. Secondly, research could also provide access to the new capabilities and advantages that systems based on flexible RF architectures are expected to have in the future.

# References


[1] D. Yavuz, "NATO and SDR", *International Software Radio Conference*, London, 2003.

[2] J. Bertrand, "Upgrading Current Radio Systems", *International Software Radio Conference*, London, 2003.

[3] E.J. Martinez, "*Transforming MMIC's*", *Proc. of Gallium Arsenide Integrated Circuit Symposium 2002, 24th Annual Technical Digest*, Oct. 2002, pp. 7-10.

[4] R. Persson, "Strategi för radioanskaffning för framtidens svenska försvarsmakt," *Presentation at Norsk-svensk radiokonferens*, Mars 2004, Lillehammer, Norge.

[5] A.S. MacLaird, "Joint Tactical Radio System", *International Software Radio Conference*, London, 2003.

[6] C. Belisle, "The software communications architecture", *International Software Radio Conference*, London, 2003.

[7] P. Darbyshire, "Implementing SDR to achieve interoperability", *International Software Radio Conference*, London, 2003.

[8] P. Eriksson, "SoCTRix Final Project Presentation Norrköping 2004-06-17," *Private Communication*, Dec. 2004.

[9] P. Eriksson et al., "Transmitter system design SoCTRix 802.11b mode," *SoCTRix Report*, In writing.

[10] P. Eriksson et al., Air Interface Requirement Specification for SoCTRix", *SoCTRix Report*, *acr011083*, rev. 1, 2003-05-23.

[11] SoCTRix Front-End pre-study report*, SoCTRix Report acr010662*.

[12] Design Report SoCTRix Tuneable Front-End Filter MPW1826, *SoCTRix Report acr012446*, rev. 1, 2003-12-15.

[13] Test Report SoCTRix Front-End Filter MPW1826, *SoCTRix Report TR_SoCTRix_Filter_MPW1826.doc*, rev. 1, 2004-05-10.

[14] R. Malmqvist et al., "Karaktärisering av aktivt front-end filter i 0.18µm RF CMOS-process," *FOI Memo 877*, 2004-05-17.

[15] R. Malmqvist et al., "Some important aspects on the design of active microwave filters using standard RF silicon process technologies," *34th European Microwave Conference*, Amsterdam, The Netherlands, Oct. 2004, pp. 941-944.

[16] A.Daleråå, "Prestudy Report SoCTRix PA SiGe", *SoCTRix Report acr010513*, rev. 1, 2003-03-12.

[17] A.Daleråå, "Design Report SoCTRix PA SiGe 1", *SoCTRix Report, acr012299*, rev. 1, 2003-11-21.

[18] A.Daleråå, "Test Report PA SiGe 2", *Wavebreaker Report,* 2004-09-17.

[19] P. Blomqvist et al., "SoCTRix – A 4G Radio Research Project – Status 2003," *Presentation at GigaHertz 2003*, Linköping, Sweden, Nov. 2003.